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**Finance**

# ANATOMY OF THE KURZWEIL FRAUD

## How Kurzweil's straight-arrow CEO went awry

On September 11, Bernard F. Bradstreet will stand before a federal judge in Boston to receive a dubious distinction accorded only a handful of his fellow Harvard business school graduates: He will be sentenced to jail.

The 51-year-old former president and co-chief executive of Kurzweil Applied Intelligence Inc. was convicted in May of masterminding an astonishingly blatant accounting fraud at Kurzweil, a small but leading-edge player in computerized speech recognition based in Waltham, Mass. With Bradstreet at the helm, the company booked millions of dollars in phony sales in the two-year period straddling its August, 1993, initial public offering. Although supposedly sold to customers, the goods instead were shipped to a local warehouse, where they gathered dust.

**BILKED INVESTORS.** To hide the scheme from outside auditors, prosecutors contended, Bradstreet and other managers forged customer signatures, altered or concealed crucial documents, and surreptitiously shifted unsold goods between warehouses. The scheme allowed Kurzweil to show profits when it was really losing substantial amounts of money, in effect bilking the investors who plowed \$24 million into the company's stock offering. When the fraud was finally exposed in mid-1994, the bottom dropped out of Kurzweil's stock. From a high of 21 in late 1993, the stock has sunk to about 2 1/2, and the company is still struggling to recover.

Despite the enormity of the chicanery and the large number of employees involved, it eluded not only auditors but also Kurzweil's outside directors and Robertson, Stephens & Co., which underwrote the IPO. In hindsight, these external watchdogs missed telltale signals, including soaring receivables. But it's often difficult to uncover fraud perpetrated by top management. And in the Kurzweil case, detection was made harder by the willingness of executives to brazenly lie and forge documents.

The involvement of Bradstreet in this sordid affair is especially bizarre. A

former Marine fighter pilot who favored short hair and buttoned-down shirts, Bradstreet struck numerous associates over his 20-year career as the epitome of an honest and straightforward executive. "He was a highly ethical family man," recalls Richard B. Goldman, a former chief financial officer at Prime Computer Inc., where Bradstreet worked as treasurer from 1979 to 1985. "Certainly, the guy I knew wouldn't knowingly perpetrate the kinds of things he has been accused of."

Indeed, Bradstreet's apparent role in the fraud seems to defy logical explanation. With his background, he should have realized that such a crude scheme would inevitably be uncovered. And the usual explanation for such events--greed--doesn't seem convincing in this case. Even had the fraud succeeded, there was no big payday in store for Bradstreet: He owned just 3.4% of the company, worth barely \$1 million at the time of the IPO.

"CLEAR-CUT CASE." On the witness stand, Bradstreet admitted the company had improperly accounted for some of its sales. But he contended the errors were the responsibility of underlings and said he didn't know about the apparent fraud until the very end. Prosecutors undermined that argument with a raft of evidence and the testimony of their star witness, former Kurzweil Treasurer Debra J. Murray. A quiet secretarial school graduate, Murray had worked closely with Bradstreet for nine years. She testified in mind-numbing detail that her former boss had directed or approved almost every step of the fraud.

Jeffrey B. Rudman, a senior attorney at Hale & Dorr in Boston who headed an investigation into the fraud for Kurzweil's outside directors, calls the scheme "the most clear-cut case with which I've ever been involved. The tragedy is that a very honorable and good man did something inexplicable in light of his history. That's what makes it so painful. What went wrong?"

Besides Bradstreet, at least 10 other employees were directly or tangentially involved. One junior accounting staffer even dummied up a phony logbook to help fool auditors, using three different inks to escape detection. Several salesmen testified they forged documents and otherwise aided in the scheme. But none of these low-level staffers were charged. Instead, prosecutors used their testimony to snare the big fish. Former Vice-President for Sales Thomas E. Campbell was found guilty of fraud and conspiracy charges alongside Bradstreet. Murray pleaded guilty and got probation.

The Kurzweil case raises the troubling question of why a group of otherwise law-abiding citizens veered into illegal behavior. One possible motivation may have been the unrelenting pressure on public companies to satisfy Wall Street's demands for steady quarterly growth. There's a huge temptation to push the accounting envelope, to enhance numbers by bending rules slightly. More than a few managers succumb to the lure and don't get caught. But how did the Kurzweil team go from bending to shattering the rules?

Unfortunately, the deepest motivations of the key players can only be surmised. Through their attorneys, Bradstreet and Campbell declined to be interviewed for this article, and Murray also demurred. But thousands of pages of trial transcript, plus interviews with numerous participants, provide

an extraordinarily detailed picture of how a promising young company derailed.

``SQUEAKY-CLEAN." The Kurzweil saga starts with the company's founder, Raymond C. Kurzweil, now 48. A computer prodigy, at age 28 he invented a machine that could scan printed material and read it aloud to the blind, using synthesized speech. In 1982, he founded Kurzweil Applied Intelligence to commercialize his speech-recognition research, in this case using computers to transform spoken words into printed text. The idea was sexy enough to attract some big-name backers, including Harvard University's endowment fund and Xerox Corp.'s venture-capital arm.

Meanwhile, Bradstreet was compiling an impressive resume. After attending Harvard College on an ROTC scholarship, he spent five years as a Marine fighter pilot and air combat instructor during the Vietnam War, becoming a captain. Then came Harvard B-school, where former classmates remember ``Brad" as hard-working and unusually devoted to his wife, Carol. ``He was honorable, decent, steady, and straight as rain, not flashy at all," recalls Marguerite A. Piret, a fellow 1974 graduate.

After a stint as a loan officer at First National Bank of Chicago, Bradstreet in 1979 took the treasurer's job at Prime. There, he struck co-workers as hyperconservative. ``Bernie was squeaky-clean," says John R. Colbert, who worked under Bradstreet as assistant treasurer. ``He didn't even swear."

Looking for a more entrepreneurial career, Bradstreet jumped to Kurzweil in 1985 as chief financial officer. At the time, the company had only a few dozen employees and almost no revenues. Bradstreet soon realized that the company's technology, though promising, was too costly and underdeveloped for the broad electronic-dictation market. Bradstreet persuaded the company to focus on the medical field, using Kurzweil gear to help doctors dictate electronic medical records. Gradually, Bradstreet took on bigger roles, first as president, then as co-CEO with Ray Kurzweil, while also retaining his CFO job. By 1991, he was in charge of all day-to-day operations.

Progress in penetrating the medical market was far slower than anticipated, in part because the technology was tricky to perfect. But by early 1992, insiders had a feeling Kurzweil was on the verge of a breakthrough. The company had moved into the black, posting a slim profit of \$111,000 in 1991 on revenues of \$10.5 million.

Both Bradstreet and Ray Kurzweil, who remained co-CEO until 1994 but was concerned chiefly with technical matters, were itching to take the company public. But according to the testimony of several Kurzweil employees, Bradstreet was convinced the company needed to post six straight quarters of improving results to make the IPO happen. Trouble was, Kurzweil's systems were a difficult sell, requiring big financial commitments from hospitals to a completely new technology.

Kurzweil's slow slide into fraud started in a fairly innocuous manner during 1991, Murray testified. If a quarter was ending but a sales rep needed a few

days to cement a sale, she said, Bradstreet began allowing the company to book the revenue a bit early. Instead of being shipped to the customer, the goods were ``temporarily" stored at a Chelsea (Mass.) warehouse called FOB America until the order was signed. Under generally accepted accounting principles, a sale can only be counted when goods leave the company's premises en route to the customer. But the maneuver was impossible to detect as long as the sale was consummated quickly.

As sales proved harder to get during 1992, the company relaxed its policy to allow sales to be booked two weeks early. And by the following year, Murray testified, the rules were stretched until ``the whole policy basically went out the window and [we did] whatever was necessary to book the revenue."

Aggressive accounting started to veer into chicanery. The turning point may have come in the final hours of Dec. 31, 1992. With the company still short of its quarterly targets, Campbell was pressuring Atlanta salesman James Hasbrouck to seal two orders from Georgia hospitals. Although Hasbrouck testified he told Campbell the customers weren't ready to sign, Campbell kept pushing, and the salesman eventually forged both customers' names on sales papers and faxed them to Campbell.

Soon after, Murray testified, Campbell came charging into her office with the \$221,000 in ersatz orders. Campbell confided to her about the forgeries, saying Hasbrouck needed more time to ``clean up the paperwork." Murray informed Bradstreet, she testified, and he told her not to worry--although Bradstreet countered in court that he didn't know about the forgeries. Murray posted the transactions.

Yet Hasbrouck never did secure the deals. Murray testified that she repeatedly asked Bradstreet what to do about the now bogus sales, but he told her to keep the sales on the books because Kurzweil ``needed to meet [a] certain revenue number in order for the public offering to continue." The equipment sat in storage until the fraud was uncovered nearly 17 months later.

Ethics experts say the decision to keep the phony revenues may have arisen from a misguided sense of loyalty. ``Executives in this type of situation often have an emotional investment in the company," says Barbara Ley Toffler, who heads an ethics consulting unit at Arthur Andersen & Co. ``They have all this wonderful stuff to offer the world. So they rationalize. They say, `We'll do this temporarily, and that will give us time to make it all come out right.' But instead, they dig themselves in deeper."

Not long after, the fakery nearly caused the scheme to prematurely unravel. As part of the annual audit, Coopers & Lybrand accountants sent letters to both customers, asking for confirmation of the orders. After Murray put pressure on Hasbrouck to find a solution, the salesman testified, he retrieved the unsigned confirmation letter from one of the customers, again forged the signature, and faxed it to the auditors. Bradstreet and Campbell knew about this maneuver, Murray testified. The unwitting auditors gave Kurzweil a clean bill of health.

With the IPO planned for the summer of 1993, the first quarter of the new fiscal year would be the final one listed in the prospectus. But once again, sales were slow, and Murray testified that Bradstreet authorized her to book another series of questionable deals.

**PAPER TRAIL.** Late on the final afternoon of the quarter, with revenues still behind target, Bradstreet made a move that for the first time linked him directly to the fraud's paper trail. To reassure another customer, Bradstreet hurriedly signed and faxed a letter that a \$450,000 order would be "contingent on our mutual agreement of the final document." This side letter meant that the customer hadn't actually agreed to buy anything. But Bradstreet told Murray to book the sale as a done deal. He never showed her the side letter, she testified, and the transaction didn't close until the following year. At the trial, Bradstreet defended his decision. But he conceded nailing down the details of the sale took longer than he expected.

On Aug. 24, the IPO finally closed. Investors paid \$10 apiece for 2.4 million shares, 35% of the company's stock. Bradstreet sold \$115,000 worth of his own shares. Although associates say Bradstreet didn't live an extravagant lifestyle, there were signs he might have needed the money. On his \$200,000 annual salary, he was paying private-school tuition for his three children. And county records show that he had been borrowing money by increasing the mortgage on his house, a five-acre spread in the tony suburb of Sudbury. The mortgage started at \$220,000 in 1983; by the early 1990s, it was up to \$448,000.

How did Bradstreet hope to get out of this mess? The most likely explanation, say outside experts, is that he was counting on a surge in revenues so the company could continue to show growth over its prior (inflated) quarterly numbers. He presumably also hoped the sales force could find customers for the excess goods sitting at FOB America.

Neither one happened. Instead, prosecutors charged that about two dozen more improperly-recorded sales were used to pump up revenues in the next three quarters of the fiscal year ended Jan. 31, 1994. Trial evidence suggests that of the \$18.4 million in sales recorded by Kurzweil that year, at least \$6.3 million should not have been included. Through it all, Bradstreet continued to present a picture of confident leadership. He hosted informal weekly lunch meetings for the entire staff and never gave a clue, say employees, that anything was other than rosy.

**PURGING FILES.** With the next big audit looming in early 1994, Murray instructed her staffers to purge files of compromising material. She testified that she also was very concerned about a transaction booked the prior July involving Florida Health Care Inc., a health maintenance organization in Daytona Beach, Fla. A marketing rep then at the HMO, David W. Spearin, had expressed interest in buying Kurzweil gear, but the deal never went anywhere. Unbeknownst to him, Kurzweil had processed a \$274,000 sale to his company--without a shred of paperwork to back it up.

Just before the audit, Murray said, she told Bradstreet they couldn't face the

auditors without a signed order from Florida Health Care. She testified that he told her to give the papers to Campbell. The next morning, they appeared in her in-box, signed "Dave Spearin." The handwriting, Murray testified, appeared to be Campbell's. After the auditors picked Florida Health Care for a confirmation letter, Murray says, Campbell again stepped in, and the letter was signed in the same handwriting.

All this came as a shock to Spearin, who says the signatures are a far cry from his usual scrawl. The whole thing, he says, "is crazy. We never even came close to buying this equipment." He, too, testified for the prosecution.

But it was a seemingly innocuous slip of paper that finally brought the curtain crashing down. On April 14, a Coopers & Lybrand staffer was routinely checking shipping invoices from FOB America when he noticed a charge for nine months' storage on an order that was supposed to have been shipped the prior April. The auditors confronted Bradstreet and Murray, who told them it must be a mistake. Undeterred, the auditors demanded a list of everything stored at FOB America. A panicked Murray said she told Bradstreet that the auditors might suddenly show up at FOB America, and they needed to move the goods to a new hiding place. The next day, the goods were shifted to a warehouse on Cape Cod.

Bradstreet's explanation was quite different. He testified that, after the auditors found the invoice, he quizzed Murray, and she told him--for the first time--about the huge amount of merchandise at FOB America. He decided to secure the goods by moving them until they could be properly accounted for. But prosecutors poked holes in this account, pointing out he failed to alert auditors or the board about the hidden computer gear.

The outside directors, meanwhile, called in Hale & Dorr to investigate. But even with auditors and attorneys crawling all over Kurzweil headquarters, Bradstreet kept his fighter-pilot cool. According to Murray, he began planning to bring the still hidden goods back to Kurzweil, hoping to pretend they had been returned by customers. Murray, however, was getting cold feet. She testified that she told Bradstreet she wouldn't help. "Isn't it a little late for that?" she recalled him replying.

TEARS. The lawyers were making little headway until they got a huge break. On May 17, Murray confessed everything in an interview with Hale & Dorr. Merriann Panarella, the Hale & Dorr attorney, vividly recalls Murray calmly producing a chart detailing every questionable transaction. It was, she recalls, "one of the most poignant moments I've ever had practicing law. Both of us were on the verge of tears."

A few days later, Bradstreet, Murray, and Campbell were forced to resign by the board. Among the casualties in the ensuing purge were Murray's entire accounting staff and most of the sales force. The scandal nearly devastated the company. Unsure whether Kurzweil would survive, customers slowed orders to a crawl.

New CEO Thomas E. Brew Jr., a crisis specialist brought in the day Bradstreet resigned, is still struggling to turn the situation around. A few

months ago, Kurzweil launched two new software products as advanced as anything on the market. Brew predicts the company will move into the black next year. ``We're confident we've put the accounting irregularities behind us," he says.

Of the top managers, only Ray Kurzweil remains with the company, albeit as chief technical officer, not co-CEO. Murray told the FBI she thought Kurzweil was aware of questionable activity, but he vehemently denied it, and prosecutors apparently concluded he had no direct involvement. Today, he says he still can't fathom why colleagues with whom he had worked closely for years could have resorted to fraud.

As for Bradstreet and Campbell, they face almost certain jail time. Sentencing guidelines call for Bradstreet to receive up to 10 years, while Campbell could get nearly six. Most observers expect the judge to be somewhat lenient, given the pair's previously spotless records. But Bradstreet, in particular, should have plenty of time behind bars to ponder a question that only he can answer: What went wrong?

*By Mark Maremont in Waltham, Mass.*

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# (WO/2007/001962) SYSTEMS AND METHODS FOR GENERATING BIOLOGICAL MATERIAL

Biblio. Data

Description

Claims

National Phase

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**Applicants:** KURZWEIL TECHNOLOGIES, INC. [US/US]; 15 Walnut Street, Wellesley Hills, Massachusetts 02481 (US) (*All Except US*).  
KURZWEIL, Raymond, C. [US/US]; (US) (*US Only*).

**Inventor:** KURZWEIL, Raymond, C.; (US).

**Agent:** MALONEY, Denis G. et al.; Fish & Richardson PC, PO Box 1022, Minneapolis, MA 55440-1022 (US) .

**Priority Data:** 60/692,327 20.06.2005 US

**Title:** SYSTEMS AND METHODS FOR GENERATING BIOLOGICAL MATERIAL

**Abstract:** The invention relates to systems and methods for synthesizing biological material.

**Designated States:** AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.  
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# Who is the world's biggest patent troll?

by [Matt Asay](#)

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In two consecutive days, *The Wall Street Journal* presented two different answers. The first is not surprising: [Intellectual Ventures](#), the brainchild of ex-Microsoft executive Nathan Myhrvold. It's now out "to [raise as much as \\$1 billion to help develop and patent inventions](#), many of them from universities in Asia." I know I will sleep so much more comfortably knowing that IVL will be out plundering Asia so that it can turn around and plunder the rest of the planet.

The second might surprise you: the University of California. The University of California may be especially pernicious because it [can sue for patent infringement but has sovereign immunity](#):

In the lucrative world of patents, the University of California is a major player. It receives by far more patents from the U.S. government than any school in the country. And by licensing out its intellectual property, the university has generated about \$500 million in revenue in the past five years.

The school also aggressively uses the courts as a sword, and is unafraid to take on big companies. As a plaintiff alleging patent infringement, the school has settled a claim against Genentech Inc. for \$200 million, secured a payment of \$185 million from Monsanto Co., and won a \$30 million settlement from Microsoft Corp.

Yet, when it comes to getting sued for patent infringement, the university, as well as the state of California, are Teflon. A legal doctrine known as sovereign immunity protects states and state institutions from legal liability. Courts have held that participating in the federal patent system doesn't cost a state its immunity. The upshot--states can sue, but effectively can't be sued.

A benevolent troll, perhaps, lovingly educating the nation's children. But one that wields a Teflon fist in a way that no patent holder should.

At least with IVL we know that it's just an avaricious troll, [whatever Myhrvold may say to the contrary](#):

Some university officials--including those from Stanford and MIT--say they aren't working with (IVL) because they worry it could use its patents for litigation or other purposes that don't promote innovation (gasp!). Myhrvold says their concern is overblown, as his company has numerous deals to buy or license patents with more than 80 universities. He says his firm simply wants to get "fair compensation" for new inventions, and help inventors do the same, and that its goal has always been to

create a more liquid IP market.

He truly is a child of Microsoft. The apple doesn't fall too far from the tree.

The University of California's patent trolling is worse, for the reasons noted above. It's an unfair advantage that should be abolished, [as Stanford Law School professor Mark Lemley argues](#):

The underlying problem is that the Supreme Court is applying an antiquated doctrine--the 11th Amendment--to circumstances in which it was never intended to apply. The Framers never contemplated states suing people for patent infringement.

At least IVL doesn't hide behind state sovereignty, though it does hide behind specious arguments as to the good it brings humanity. Something is clearly wrong when a state can stripmine the IP landscape with impunity.



Matt Asay is chief operating officer at Canonical, the company behind the Ubuntu Linux operating system. Prior to Canonical, Matt was general manager of the Americas division and vice president of business development at Alfresco, an open-source applications company. Matt brings a decade of in-the-trenches open-source business and legal experience to The Open Road, with an emphasis on emerging open-source business strategies and opportunities. He is a member of the CNET Blog Network and is not an employee of CNET. You can follow Matt on [Twitter @mjasay](#).

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**(WO/2008/063473) NANOROBOTICS SYSTEM**[Biblio. Data](#)[Description](#)[Claims](#)[National Phase](#)[Notices](#)[Documents](#)

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60/912,133 16.04.2007 US**Title:** NANOROBOTICS SYSTEM**Abstract:** The invention pertains to hybrid control systems for collectives of nanorobots that exhibit intelligence, social behavior and environmental interaction. The collectives of nanorobots (CNRs) use software agents and metaheuristics, such as hybrid genetic algorithms, to solve optimization problems in evolving environments involving resource constraints.**Designated States:** AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.  
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## DEPARTMENTS

## Art Fraud Forensics

## An engineer helps curators foil forgers

BY SUSAN KARLIN // JULY 2009

How many engineering jobs let you take a van Gogh off the wall and hold it in your hands? The kind C. Richard Johnson Jr. landed. He's both an electrical engineering professor at Cornell University, in Ithaca, N.Y., and an adjunct research fellow at the Van Gogh Museum, in Amsterdam. As such, Johnson says, he can "speak the language of people on both sides."

And when the two sides talk, they mainly talk about fraud and how to detect it. Two years ago, Johnson organized a conference at the museum that brought together researchers from Pennsylvania State University and Princeton, in the United States and Maastricht University in the Netherlands. Together, they processed high-resolution images with specially designed signal-processing algorithms to help sort fake van Goghs from real ones at the brushstroke level. It was the first time that image-processing teams at different universities could compare authentication approaches on the same paintings. Another workshop will follow next year at the Museum of Modern Art, in New York City.





PHOTO: VAN GOGH MUSEUM

**Painting by numbers:**

C. Richard Johnson [left, center] uses signal-processing algorithms to authenticate canvases believed to be painted by van Gogh.

"Fraud detection is a 'sexy' topic, which is why it was an early focus of my activities," says Johnson. "But we're 10 to 15 years away from the computer having any authority in it. So now my colleagues and I are pursuing a wide variety of issues of interest to conservators and art historians, where signal processing can provide assistance that reaches well beyond just the detection of frauds."

Johnson's current focus is on canvas thread counts—the number of horizontal threads

crossing a vertical line 1 centimeter long—to identify paintings from the same roll of canvas. "Placing a questioned painting on the same canvas roll as a painting known to be from a particular artist supports authentication to an artist who bought canvas in rolls, as van Gogh often did," he says. "When canvas is prepared with a lead white ground, the grooves between the threads are filled with radio-opaque material," says Johnson. "This registers in an X-ray as an intensity pattern that reveals the individual threads, permitting a calculation of the weave density." The pattern is then analyzed with a Fourier transform, the same technique that radio engineers use to break down a signal into a series of simple sine waves.

The team is distributing the software free to museums. The Van Gogh Museum already uses the data generated to identify paintings from the same canvas roll by determining how the sections were arranged on the roll before being cut for use.

Johnson stumbled into art as he wandered through Berlin museums during a college year abroad while earning a bachelor's in electrical engineering from Georgia Tech. Later, while working on his Ph.D. in EE at Stanford, he took a class in the Dutch masters, which rekindled his passion. In 1977, he became the first Ph.D. student to graduate from the university with a minor in art history.

He went straight into academia, teaching at Virginia Tech until 1981, when he moved to Cornell. He was named an IEEE Fellow in 1989 for his work in digital control and signal processing.

"This kind of research is not something to recommend to Ph.D. students. There are no jobs, no one's eager to fund this, and it's career killing for any pretenure academic," he says, laughing. "But for me, it's like having a backstage pass. I go to a conservation studio and can take a van Gogh out of its frame and examine it."

**About the Author**

Susan Karlin lists among her achievements acting, drawing, traveling to every continent on Earth, and writing for publications such as The New York Times, Entertainment Weekly, and Spectrum. For this issue she follows the trail of a coffee-making cellphone in "Phone-y Brew" [p. 22] and reports on an electrical engineer who helps museums spot fake van Goghs in "Art Fraud Forensics" [p. 23].





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**Solomon, Neal**  
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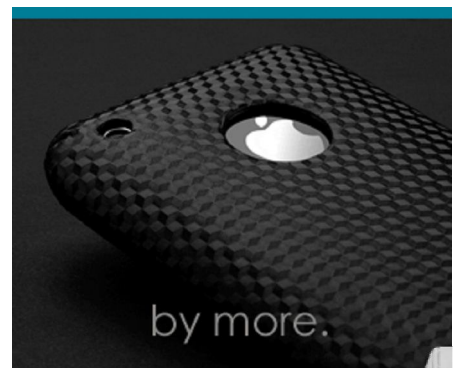
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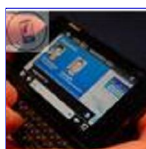
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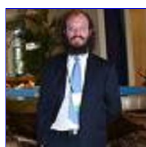
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... developed for mobile browsers but has now been made available, via an API, for a range of devices including Macbooks, Thinkpads and **Linux** machines. ...

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SDTimes.com - [Alex Handy](#) - 10 hours ago

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As part of our deal you'll also see partially cloned **Linux** reviews appearing here on ET. I've always suspected that Lance might be a bit on the dotty side ...



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[Red Hat Shares Rise After Reporting 2Q Profit >RHT](#) Wall Street Journal

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Overview: Red Hat Enterprise **Linux** has been designed by, and for, the most security-conscious organizations in the world. Accordingly, security has always ...

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[Microsoft Working With Red Hat \*\*Linux\*\* to Increase Virtual Server Interoperability](#)

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And it's currently only available with Windows XP, even though Asus was a pioneer in putting **Linux** on netbooks. But this weekend Asus did something ...

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In addition to now being able to discover, monitor, provision, and patch Oracle Enterprise **Linux** on x64 iron, the Sun management tool can now create, ...

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InformationWeek - [Marin Perez](#) - Sep 23, 2009

The chipmaker added phone and social networking functionality to its **Linux**-based operating system, paving its way into smartphones. ...

[Intel Presents the Moblin Linux Software for Smartphones](#) High Tech Lounge

[Intel Hints at Its Own Smartphone Operating System](#) Wired News

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[World of Goo on sale, plus iPhone version coming](#) InfoWorld

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If anyone needed further confirmation of Cisco's software aspirations, its forays into **Linux** offer a strong hint. In what might have looked like a publicity ...

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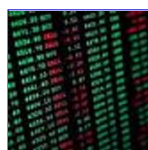
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Upon application to the Patent Office and compliance with the requirements of the Patent Act,<sup>1</sup> an inventor is granted<sup>2</sup> the right to prohibit others from manufacturing, selling, or using an invention claimed in a patent.<sup>3</sup> Although the Patent Office attempts to develop information relevant to each application, limited resources<sup>4</sup> and lack of access to relevant unpublished data force it to rely heavily on information submitted by applicants.<sup>5</sup> Even when disclosure is candid and complete, the Office sometimes issues patents that should not have been issued. The chances of error are obviously increased when an applicant

<sup>1</sup> 35 U.S.C. §§ 1 *et seq.* (1970). The subject matter covered by the patent must be a "process, machine, manufacture, or composition of matter, or . . . improvement thereof," *id.* § 101, which is "new and useful," *id.*, and not obvious from the prior art in the field, *id.* § 103. The applicant must be the first inventor and must not have lost or abandoned the right to a patent, *id.* §§ 102(c), (f). The application must describe the invention in sufficient detail to enable one skilled in the relevant art to make and use the invention, *id.* § 112, and the portion of the described matter that constitutes the invention must be distinctly claimed, *id.* § 112. An applicant may appeal an initial rejection of his application through the Patent Office and, if necessary, to the courts, *id.* §§ 134, 141, 145 & 146.

<sup>2</sup> The Patent Office usually evaluates the merits of a patent application in *ex parte* proceedings. Ladd, *Business Aggression Under the Patent System*, 26 U. CHI. L. REV. 353, 356 (1959). When it appears that two or more pending applications cover the same invention, the question of which applicant was the first inventor is decided in an adversary proceeding known as an interference. 35 U.S.C. § 135; 37 C.F.R. §§ 1.201, 1.212 (1973).

<sup>3</sup> 35 U.S.C. § 154 (1970). The grant must be temporary, U.S. CONST. art. I, § 8, and currently extends for seventeen years. 35 U.S.C. § 154 (1970). A patent holder can issue licenses under a patent or transfer all rights by assignment of the patent. *Id.* § 261; see *Bement v. National Harrow Co.*, 186 U.S. 70, 88-89 (1902). Unless otherwise noted, this comment considers only original patentees. A patentee can enforce patent rights in an infringement action. The court can award various remedies: damages or treble damages for past infringement, 35 U.S.C. § 284; see *American Safety Table Co. v. Schreiber*, 415 F.2d 373 (2d Cir. 1969), *Cert. denied*, 396 U.S. 1038 (1970); an injunction against further infringement, 35 U.S.C. § 283; and, in exceptional cases, attorney's fees. *Id.* § 285.

<sup>4</sup> The situation has not changed appreciably since Learned Hand noted: "Examiners have neither the time nor the assistance to exhaust the prior art; nothing is more common in a suit for infringement than to find that all the important references are turned up for the first time by the industry of a defendant whose interest animates his search." *Rosenberg v. Groov-Pin Corp.*, 81 F.2d 46, 47 (2d Cir. 1936). See generally *Graham v. John Deere Co.*, 383 U.S. 1, 18 (1966); *Norton v. Curtiss*, 433 F.2d 779, 794 (C.C.P.A. 1970); Ladd, *supra* note 2.

<sup>5</sup> See Ladd, *supra* note 2, at 356-57.

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## Patent application title: **System, methods and apparatuses for integrated circuits for nanorobotics**

**Inventors:** [Neal Solomon](#)

**Agents:** [Neal Solomon](#)

**Assignees:** [Solomon Research LLC](#)

**Origin:** [OAKLAND, CA US](#)

**IPC8 Class:** [AG06F1750FI](#)

**USPC Class:** [716 16](#)

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### Abstract:

The invention describes apparatuses for nano-scale integrated circuits applied to nanorobotics. Using EDA techniques, the system develops fully functional nano ICs, including ASICs and microprocessors. Three dimensional nano ICs are disclosed for increased efficiency in nanorobotic apparatuses. Nano-scale FPGAs are disclosed. The nano-scale semiconductors have applications to nano-scale and micro-scale robots.

### Claims:

1. A system for organizing a nano-scale semiconductor, comprising:a layer of hafnium substrate;a series of rows of nano-scale transistors in arrays on the substrate;routing logic arrays by using nano-scale connectors between the transistors;routing memory arrays by using nano-scale connectors between the transistors;wherein the logic arrays are structured into ASIC or MP devices;wherein the logic arrays are organized by using EDA layout software;wherein the semiconductor device has between 4,000 transistors and 20,000 transistors in a two dimensional configuration; andwherein the logic arrays contain a multiply-accumulate-convert (MAC) component.
2. The system of claim 1:wherein the device is layered with three to fifteen layers;wherein the layers are connected with through silicon vias (TSVs);wherein the layers contain tiles with specific functionality;wherein the logic arrays are structured into ASIC, MP or hybrid devices;wherein the logic arrays are organized by using EDA layout software;wherein the semiconductor device has between 20,000 transistors and 100,000 transistors in a two dimensional configuration; andwherein the logic arrays contain a multi-accumulate-convert (MAC) component.
3. The system of claim 1:wherein a series of rows of nano-scale gates are arrayed on the substrate;wherein the routing of logic arrays is done by using nano-scale connectors between the gates;wherein the gates are structured into grids of evolvable logic arrays;wherein the logic array grids access look up tables (LUTs) on the periphery of the device;wherein the logic array grids access memory on the periphery of the device;wherein the gates configure to a different position when initiated;wherein the device contains between 1,000 and 10,000 gates; andwherein the device reconfigures its gates in response

to feedback from its environment.

**4.** A system for organizing multiple nano-scale FPGAs, comprising: a network of nano-scale FPGAs that communicate with each other by linkage in a network; wherein the network of nano-scale FPGAs coordinate their behaviors; wherein the network of nano-scale FPGAs receive inputs from an indeterministic environment; wherein the network of nano-scale FPGAs analyze the inputs from the indeterministic environment; wherein the network of nano-scale FPGAs restructure their configurations to optimally respond to the environment; and wherein the network of nano-scale FPGAs continue to update their restructuring to the most recent environmental changes.

**5.** A system for organizing a nano-scale semiconductor in a nanorobotic device, comprising: a layer of hafnium substrate; a series of rows of nano-scale transistors in arrays on the substrate; routing logic arrays by using nano-scale connectors between the transistors; routing memory arrays by using nano-scale connectors between the transistors; wherein the semiconductor is installed into the nanorobotic device; wherein the semiconductor device is organized to analyze data and receive data inputs from sensors; wherein the semiconductor device is organized to send and receive signals by using a communications component; and wherein the semiconductor device activates an actuator in the nanorobot.

## **Description:**

## **CROSS-REFERENCES TO RELATED APPLICATIONS**

**[0001]** The present application claims the benefit of priority under 35 U.S.C. § 119 from U.S. Provisional Patent Application Ser. No. 60/865,605, filed on Nov. 13, 2006 and U.S. Provisional Patent Application Ser. No. 60/912,133, filed Apr. 16, 2007, the disclosures of which are hereby incorporated by reference in their entirety for all purposes.

## **FIELD OF THE INVENTION**

**[0002]** The present invention pertains to the field of nanotechnology and nanorobotics. The system deals with epigenetic robotics applied to collectives of nanorobots. Specifically, the invention relates to nanoelectromechanical systems (NEMS), microelectromechanical systems (MEMS) and nanomechatronics. The invention also deals with the coordination of collectives of nanorobots and synthetic nanorobots, including synthetic assemblies of NEMS and synthetic nano-scale and micron-scale machine assembly processes. Applications of these systems and processes are made to nanoelectronics, bionanotechnology and nanomedicine.

## **BACKGROUND OF THE INVENTION**

**[0003]** To date, four waves, or generations, of nanotechnology have evolved. The first generation was comprised mainly of developments involving chemical composition, such as new nanomaterials. The second generation developed simple tubes and filaments by positioning atoms from the ground up with novel machinery. The third generation developed nanodevices that perform specific functions, such as nanoparticles for the delivery of chemicals. Finally, the fourth wave has developed self-assembling nanoentities by chemical means.

**[0004]** The present invention represents a fifth generation of self-organizing collectives of intelligent nanorobotics. Self-organizing processes are possible at the nano- and micron-level because of the convergence of nanoelectronics developments and nanomechatronics developments.

**[0005]** While the first four generations of nanotechnology have been developed by theoretical scientists and inventors, the fifth generation of nanotechnology has been largely open until now. The present invention fills the gaps in the literature and in the prior art involving nanorobotics.

**[0006]** Early twentieth century theoretical physicists discovered that the simplest atoms were measurable at the nanometer scale of one billionth of a meter. In 1959, in his lecture "Race to the Bottom," the physicist Richard Feynman proposed a new science and technology to manipulate molecules at the nanoscale. In the 1970s Drexler's pioneering research into nanotechnology molecular-scale machinery provides a foundation for current research. In 1979, researchers at IBM developed scanning tunneling microscopy (STM) with which they manipulated atoms to spell the letters IBM. Also in the 1970s Ratner and his team at Northwestern developed the first nano-scale transistor-like device for nanoelectronics, which was developed into nanotransistors by researchers at the University of California at Berkeley in 1997. Researchers at Rice, Yale and Penn State were able to connect blocks of nanodevices and nanowires, while researchers at Hewlett Packard and UCLA were able to develop a computer memory system based on nanoassembly. Additionally, government researchers at NASA, NIST, DARPA and Naval Research have



ongoing nanotechnology development projects, though these are mainly focused on nanoelectronics challenges. Finally, researchers at MIT, Cal Tech, USC, SUNY, Cornell, Maryland, Illinois and other universities in the U.S. have been joined by overseas researchers in developing novel nanotechnologies in order to meet Feynman's challenge.

**[0007]** Nanotech start-up ventures have sprung up to develop nanoscale crystals, to use as biological labels, for use in tagging proteins and nucleic acids (Quantum Dot) and to develop micro-scale arms and grippers by using MEMS to assemble manufacturing devices (Zyvex). Additionally, Nanosys, Nanometrics, Ultatech, Molecular Electronics, Applied Nanotech and Nanorex are ventures that have emerged to develop products in the nanotechnology market space. Until now, however, most of these businesses have focused on inorganic nanomaterials. Though a new generation of materials science has been aided by these earlier generations of nanotechnologies, the real breakthrough lies in identifying methods of developing intelligent systems at the nano-scale.

**[0008]** The two main models for building nanotechnology applications are the ground up method of building entities, on the one hand, and the bottom down method of shrinking photolithography techniques to the nanoscale. Both models present challenges for scientists.

**[0009]** In the case of the bottom up models, several specialized tools have been required. These include (a) atomic force microscopy (AFM), which uses electronics to measure the force exerted on a probe tip as it moves along a surface, (b) scanning tunneling microscopy (STM), which measures electrical current flowing between a scanning tip and a surface, (c) magnetic force microscopy (MFM), which uses a magnetic tip that scans a surface and (d) nanoscale synthesis (NSL), which constructs nanospheres.

**[0010]** In the case of the top down models, several methods and techniques have been developed, including (a) x-ray lithography, (b) ion beam lithography, (c) dip pen nanolithography (DPN), in which a "reservoir of `ink` (atoms/molecules) is stored on top of the scanning probe tip, which is manipulated across the surface, leaving lines and patterns behind" (Ratner, 2003) and (d) micro-imprint lithography (MIL), which emulates a rubber stamp. Lithography techniques generally require the creation of a mask of a main model, which is then reproduced onto a substrate much like a semiconductor is manufactured. It is primarily through lithographic techniques that mass quantities of nanoentities can be created efficiently and cost-effectively.

**[0011]** The main patents obtained in the U.S. in the field of nanotechnology have focused on nanomaterials, MEMS, micro-pumps, micro-sensors, micro-voltaics, lithography, genetic microarray analysis and nano-drug delivery. Examples of these include a meso-microelectromechanical system package (U.S. Pat. No. 6,859,119), micro-opto-electro-mechanical systems (MOEMS) (U.S. Pat. No. 6,580,858), ion beam lithography system (U.S. Pat. No. 6,924,493), carbon nanotube sensors (U.S. Pat. No. 7,013,708) and microfabricated elastomeric valve and pump systems (U.S. Pat. Nos. 6,899,137 and 6,929,030). Finally, patents for a drug targeting system (U.S. Pat. No. 7,025,991) and for a design of artificial genes for use as controls in gene expression analytical system (U.S. Pat. No. 6,943,242), used for a DNA microarray, are applied to biotechnology. For the most part, these patents represent third and fourth generation nanotechnologies.

**[0012]** A new generation of nanotechnologies presents procedures for objects to interact with their environment and solve critical problems on the nano- and micron-scale. This generation of technology involves social intelligence and self-organization capabilities.

**[0013]** Biological analogies help to explain the performance of intelligent or self-organizing nanoentities. In the macro-scale environment, the behaviors of insects provides an important model for understanding how to develop models that emulate social intelligence in which chemical markers (pheromones) are used by individual entities to communicate a social goal. On the micro-scale, microbes and pathogens interoperate with the animal's immune system, in which battles either won or lost determine survival of the host. Other intracellular models show how proteins interact in order to perform a host of functions. At the level of DNA, RNA transcription processes are highly organized methods for developing cellular reproduction. These micromachinery processes and functions occur at the nanoscale and provide useful analogies for nanotechnologies.

**[0014]** In order to draw on these biological system analogies, complexity theory has been developed in recent years. Researchers associated with the Sante Fe Institute have developed a range of theoretical models to merge complexity theory and biologically-inspired processes, including genetic algorithms and collective behavior of economic agents.

**[0015]** Such a new nanotechnology requires distributed computation and communication techniques. It is, moreover, necessary for such a technology to adapt to feedback from its environment. The present invention presents a system in which these operations occur and specifies a range of important applications for electronics, medicine and numerous other areas. The main challenges to this advanced nanotechnology system lie in the discovery of solutions to the problems of limited information, computation, memory, communication,



mobility and power.

## **[0016]Challenges**

**[0017]**The development of a fifth generation of nanotechnologies faces several challenges. First, the manufacturing of nanoparticles is difficult. Second, the assembly of nanoparticles into functional devices is a major challenge. Third, the control and management of nanosystems is complex. Since physical properties operate differently at the nano-scale than at the macro-scale, we need to design systems that accommodate these unique physical forces.

**[0018]**The problems to identify include how to: **[0019]**Build nanorobots **[0020]**Connect nanodevices **[0021]**Develop a nanorobotic power source **[0022]**Develop nanorobotic computation **[0023]**Develop specific nanorobotic functionality **[0024]**Develop nanorobotic communication system(s) **[0025]**Develop multi-functional nanorobotics **[0026]**Activate nanorobotic functionality **[0027]**Develop nanorobotic computer programming **[0028]**Develop an external tracking procedure for a nanorobot **[0029]**Develop an external activation of a nanorobot **[0030]**Develop a hybrid control system for nanorobots **[0031]**Use AI for nanorobots **[0032]**Obtain environmental inputs via sensors

## **[0033]Developing Solutions to these Problems**

**[0034]**Most prior technological innovations for nano-scale problems have focused on the first generations of nanotechnology and on materials science. The next generation focuses on intelligent systems applied to the nano entities. This fifth generation of innovation combines the development of nano-scale entities with intelligence of complex systems.

**[0035]**Few researchers have devised solutions to these complex nano-scale problems. Cavalcanti has developed theoretical notions to develop a model of nanorobotics. However, these solutions are not practical and will not work in real situations. For example, there is not enough power of mobility in this model to overcome natural forces. Similarly, according to this theoretical approach, autonomous computation resources of nanorobots are insufficient to perform even the simplest functions, such as targeting. Without computation capacity, AI will not work at this level; without AI there is no possible way to perform real-time environmental reaction and interaction.

**[0036]**Cavalcanti's 2D and 3D simulations are dependent on only several variable assumptions and will not withstand the "chaos" of real environmental interactive processes. In addition, the structure of these nanorobots cannot be built efficiently from the bottom up and still retain critical functionality. Even if these many problems can be solved, individual nanorobots cannot be trusted to behave without error inside cells.

**[0037]**The emerging field of epigenetic robotics deals with the relations between a robot and its environment. This field suggests that it is useful to program a robot to learn autonomously by interacting with its environment. However, these models do not apply to groups of robots in which it is necessary to learn from and interact with many more variables in the robots' environment, including societies of other robots. In the case of groups of nanorobots with resource constraints, the present invention adds volumes to this promising field.

**[0038]**Solomon's research in developing hybrid control systems for robotic systems and in developing novel approaches for molecular modeling systems presents pathways to solving these complex problems. These novel research streams are used in the present invention.

**[0039]**Prior systems of robotics generally do not address the complexities of nanotechnology. The behavior-based robot system using subsumption methods developed by Brooks at MIT is useful for managing individual robot behavior with limited computation capacity. On the other end of the spectrum, central control robotic systems require substantial computation resources. Hybrid control robotic systems synthesize elements from these two main control processes. Even more advanced robotic control systems involve the integration of a multi-agent software system with a robotic system that is particularly useful in controlling groups of robots. This advanced robotic control system experiences both the benefits and detriments of the behavior-based model and the central control model.

## **[0040]The Nanorobotic Environment**

**[0041]**The nano domain, which is a billionth of a meter, is measured in millionths of a meter. A single oxygen atom is roughly a single nanometer across. A micron is a millionth of a meter. The width of a human hair is about 60,000 nanometers.

**[0042]**The present invention focuses on the synthetic development of objects that are in a middle (meso-nano) sphere somewhat between the atomic size (micro-nano) of simple atoms and the mega-nano domain of micron-sized objects. While it is true that scientists have built, from the ground up, that is, atom by atom, objects such as elegant geodesic

nanotubes made of carbon atoms, objects in this domain are too small and too expensive to construct to be useful for an active intelligent system. In order to be useful, a nanorobotic system requires numerous and economical robots dependent on mass production techniques that must generally be considered from the perspective of a top down strategy, that is, by utilization of largely lithographic procedures.

**[0043]**The nanorobotic entities described herein generally consist of objects with dimensions from 100 nm to 1000 nm (1 micron) cubed, but can be smaller than 100 nm or larger than ten microns. This size is relatively large by nanotechnology standards, but is crucial in order to maintain functionality. Keep in mind that a white blood cell is comprised of about 100,000 molecules and fits into this meso-nano domain. The micron-scale space of inter-object interaction may be comprehended by analogy to a warehouse in which nanoscale objects interact. In order to be useful, nanorobots require complex apparatus that includes computation, communications, sensors, actuators, power source and specific functionality, all of which apparatus requires spatial extension. Though this domain specification is larger than some of the atomic-scale research in nanotechnology, it is far smaller than most microelectronics.

**[0044]**While the larger meso-nano assemblies described herein possess a specific geometric dimensionality, the size dimensions of the domains in which they operate are also critical to consider. In these cases, each application has a different set of specifications. In the case of the human body, specific cells will have a dimensionality that is substantially larger than the complex molecular-size proteins that are constructed for interoperation within them.

**[0045]**Over time, however, it will be possible to make very small, useful micro-nano scale robots for use in intelligent systems. Thus, we may conceive of several generations of scale for these systems, the first being in the meso-nano domain.

## **SUMMARY OF THE INVENTION**

**[0046]**The invention specifies nano-scale integrated circuits (ICs) with applications to nanorobotic electromechanical devices. The nano-ICs have microprocessor, ASIC or FPGA architectures. The IC architectures include computer memory, MAC components and interconnects that are designed with EDA software. The system also specifies nano-scale system on chip architectures.

**[0047]**The invention disclosed a class of nano-scale three dimensional ICs. By stacking layers of ICs onto 3D chips using through silicon vias (TSVs) and multilayer CMOS fabrication techniques, the nano-MPs, nano-ASICs and nano-FPGAs of the present invention maximize performance and efficiency.

**[0048]**The chips are applied to nanorobotics. By integrating nano-scale ICs into nanorobots, the nanorobot devices obtain intelligence functionality that includes data analysis, memory access, sensor access, communications control and mobile control.

**[0049]**The ICs process program code by employing software agents and by interacting with external computation. Specifically, the system uses genetic algorithms and reduced instruction AI techniques to overcome computing resource constraints.

**[0050]**The present system is also applied to microrobots and to devices that integrate MEMS.

**[0051]**Advantages of the Invention

**[0052]**Use of nano-scale ICs provide intelligence functionality to nanorobots and microrobots.

**[0053]**By combining multiple nanorobots into collectives, the use of nano-scale ICs allow grid computing capabilities that allow social intelligence capabilities with numerous applications to electronics and biology.

## **DESCRIPTION OF THE INVENTION**

**[0054]**(I) Integrated Circuits in Nano-Robots

**[0055]**In order to achieve intelligence, it is necessary for nano-scale and micron-scale robotic entities to embody integrated circuits. While trends in ICs have focused on generating the fastest chips with billions of transistors, the current system seeks to develop extremely small, yet highly functional, circuits for use in nanorobots. By interoperating with multiple nanorobots, the intelligent robots are organized into collectives similar to the grid computing paradigm.

**[0056]**One main model for nanorobotic ICs is the traditional two dimensional chip approach which employs microprocessor architectures, such as RISC, ASIC and complex

programmable logic device (CPLD), such as FPGA architectures. This model integrates logic and memory components using traditional interconnects onto devices in different chip configurations according to each application preference.

**[0057]** Another model employs a new generation of efficient three dimensional IC architectures. This approach stacks layers of ICs by using through silicon vias (TSVs) to connect the layers. This model is useful to create micron-scale and nano-scale 3D system on chip (SoC) technologies that are applicable to nanorobotics. This approach leads to the system on a nano chip (SONC) model disclosed herein.

**[0058]** Because the model employs multiple nanorobots in collectives in order to be functionally useful, the present invention uses heterogeneous computing options to maximize functionality. For example, collectives of nanorobots are comprised of nanorobots that include multiple types of ICs, including ASICs, MPs, FPGAs and active storage devices that integrate logic and memory in different ways in order to optimize specific tasks. By working together in collectives using a division of labor enabled by multiple computing types, the present system maximizes computability at the ultra small scale.

**[0059]** Micron-scale computing exists. Hitachi has produced a family of micron-scale chips that measure 0.4 mm squared. The "super-micro" chips are used for radio frequency identification (RFID) applications. Since they contain read only memory exclusively, their functionality is highly restricted.

**[0060]** However, with the advent of smaller transistors made possible by novel lithographic techniques, next generation ICs will be capable of very small size. In a sense, rather than seeking ever faster computing capability with more and more transistors in order to maintain Moore's law, the present system seeks to go back to the origins of the integrated circuit.

**[0061]** The first microprocessors, such as the Intel 8080, used only 4500 transistors and were capable of 200K operations per second. The Motorola MC6800 used 200K transistors and achieved substantial functionality.

**[0062]** The present system is able to achieve capabilities between 4,000 and 1,000,000 transistors within nano-scale and micron-scale integrated circuits, respectively, in both 2D and 3D embodiments, in order to be useful within nanorobots and micron-scale robots.

**[0063]** While 45 nm transistors are used in ICs, 32 nm, 26 nm, 22 nm, 16 nm and 10 nm scale transistors have been constructed using novel lithographic techniques. For 22 nm transistors high index immersion lithography is used and for 16 nm transistors high index immersion lithography is combined with double patterning techniques. 10 nm and 16 nm transistors are comprised of 3D fin field effect transistors (FETS). These classes of ICs are designed using CMOS fabrication techniques.

**[0064]** (1) Nano-scale Integrated Circuit for Nanorobots using EDA Processes

**[0065]** Electronic design automation (EDA) techniques are used in the chip architectural process. Transistors are organized in logic and memory components of integrated circuits by using layout and routing of interconnects with EDA.

**[0066]** Nano-scale ICs are designed as simple modular combinations of logic and memory components. By organizing a family of N-ICs, EDA techniques develop optimal options with 4,000 to 10,000 transistors. These small chip options, whether ASIC, FPGA microprocessor or hybrid, deliver multiple functionality for nanorobots. Very simple MP functionality is supplemented by combining multiple nanorobots into collectives that share computation, communications and software.

**[0067]** Chips at the submicron scale are designed in CMOS by using lithographic fabrication techniques. The 2D model N-IC results in "flat" chips that are useful in some nanorobotic applications, particularly for the simplest computational functions.

**[0068]** These chips contain 16-bit or 32-bit RAM and 256-byte or 512-byte ROM memory components and are capable of 8-bit, 16-bit or 32-bit computation functionality.

**[0069]** Because they are SoNCs, they also contain analog functionality (ADC and DAC), sensors and communications functionality on the chip as well as logic and memory capability.

**[0070]** (2) Three Dimensional Nano-IC for Nanorobots

**[0071]** Three dimensional ICs possess increased functionality in an efficient space than traditional 2D ICs. 3D chips stack 2D layers of ICs and are constructed using CMOS layering techniques in fabrication. The 3D chip architecture allows organization of memory and logic on tiles of each layer and thereby increases the options for chip design in order to optimize chips for multiple applications. These hybrid N-ICs provide an ideal application to

nanorobotics.

**[0072]**By constructing a layer of a 3D N-IC with 26 transistors by 26 transistors, or 676 transistors on a single layer, and by stacking eight layers using CMOS technology, the 3D N-IC are comprised of a total of 5408 transistors, yet are contained in a compact space with an 4:1 aspect ratio. Only a small deviation of one less transistor per row yields a 25 by 25 transistor layer (525 transistors on a single layer) and 4200 transistors on an 8 layer N-IC.

**[0073]**In substantially larger 3D N-IC chips, 200 transistors by 200 transistors comprise a single layer of 40K transistors, with a total of 200K transistors in a 5 layer N-IC. With an average transistor size of 22 nm (averaging 16 nm and 26 nm), the total space used is approximately 4400 nm squared (19,360,000 nm square). This chip is capable of 6 MIPS. Similarly, using 100 by 100 transistors yields a 10,000 transistor layer. Nine layers of this chip produces a 90K transistor 3D N-IC capable of 3.6 MIPS. This chip is approximately 2200 nm squared (4,840,000 nm square). Finally, 258 by 258 transistors produces 66,666 transistors per layer. Stacking 12 layers produces an 800K transistor meso N-IC device capable of 24 MIPS.

**[0074]**3D N-ICs may be MPs, ASICs, FPGAs, active storage devices or hybrids.

**[0075]**(II) Nano-scale FPGAs

**[0076]**Field programmable gate arrays (FPGAs) are either deterministic or indeterministic. Deterministic FPGAs are used to oscillate between various application specific integrated circuit positions in order to adapt to a changing environment. Indeterministic FPGAs will operate continuously until they solve a particular problem. These continuously programmable FPGAs (CP-FPGAs) are used for rapid prototyping in the field thereby enabling them to interact with an evolving environment.

**[0077]**(1) Nano-FPGAs (N-FPGAs)

**[0078]**Given the steady increase in semiconductor speed and steady decrease in size, the design of nano-scale FPGAs is achievable.

**[0079]**The present invention specifies an FPGA in which there is continuous transformation of the configuration of the gate arrays in order to solve problems at the nano-scale. Among other applications, N-FPGAs will be used within nano-robots in order to more rapidly interact with an evolving environment. While N-FPGAs are used within the nanorobots to provide computational functionality, the gates of the N-FPGAs are comprised of nano-scale objects and interconnects.

**[0080]**Since the N-FPGA is indeterministic in order to maintain maximum functionality in evolutionary environments, it is necessary to have a way to track the record of its evolution. The present system therefore has a mechanism to track the evolvability pattern of the N-FPGA in order to record its transformational pathways by exporting its sequential evolution of structural transformation to an external computer for analysis. This method of tracking the indeterministic N-FPGA, by using communications links and modeling processes, eliminates the need to reverse-engineer the specific pattern of the evolution of the gate structures over time. By creating a communications interface that tracks the gate structure evolution process using an external computer, the system provides additional environmental data and activates the N-FPGA by employing external macro-computation as well.

**[0081]**(2) Evolutionary N-FPGAs

**[0082]**Because they are comprised of nano-scale parts, N-FPGAs "evolve" on-demand by combining autonomous programmable modular components and logic arrays in order to expand functionality. For example, this autonomous modularity of components facilitates whole memory sections of a chip while the chip is operational. This allows a new dimension of nano-scale evolvable hardware (N-EHW) in which whole new sections of the chip autonomously evolve. This embodiment of the present invention is critical in order to establish self-repairing hardware on the nano- and micron-scale. With this process it is possible to engage in the limited replication of a semiconductor in the field, for the purpose of repairing hardware. This view presents an embryonic model of electronics N-EHW. The development of a micro-scale artificial brain is a consequence of this view of evolutionary semiconductors.

**[0083]**By using the N-EHW CNR features of self-assembly and reaggregation, the present invention provides methods for FPGAs' to add sections and functional capacity akin to an evolving artificial brain. This would be similar to the development of a brain from a child to that of an adult in which the modular aggregated N-FPGA network co-adapts to its evolving environment and constantly learns as it grows in order to continually optimize its performance.

**[0084]**(3) Networks of N-FPGAs

**[0085]** Networks of N-FPGAs operate within a CNR system. The N-FPGAs have external linkages between nanorobot nodes. The N-FPGAs are the artificial brains of the nanorobots and are linked together into a network by a communications system that uses software agents in a multi-agent system. In networks of N-FPGAs in CNRs, the nanorobots that are not functional represent bottlenecks around which the network reroutes communications. The N-FPGA and CNR network achieves a level of operational plasticity by constantly rerouting its arrangement in order to optimize solutions.

**[0086]** By linking together the N-FPGAs into a computer network, the computational capacity of the CNR system substantially increased.

**[0087]** In another embodiment of the present system, N-FPGAs are not contained within the nanorobots, but rather function as central modules CNRs may access. These micro-FPGAs are centralized for use by a single CNR team or a combination of teams. These FPGAs behave as the main computer server for the multitude of nanorobots in the collective. The FPGAs appear as centralized modules that are physically adjacent to the CNR teams.

**[0088]** In yet another embodiment of the system, micro- or nano-FPGAs are replaced by micron- or nano-scale microprocessors.

**[0089]** In still another embodiment of the invention, the system uses external computing resources that are accessed through the communication system by the use of software agents.

**[0090]** (4) Interaction of N-EHW CNRs and N-FPGAs

**[0091]** One of the main advantages of utilizing FPGAs is to adapt the hardware to an environment based on feedback from the environment as it changes. Similarly, the advantage of the N-EHW is to adapt to feedback from an evolving environment.

**[0092]** The feedback from, and adaptation to, the environmental changes activate the transformational processes of both the N-FPGAs and the N-EHWs. The new position of the N-EHW apparatus then transforms its configuration and accepts new information from the environment and continues to transform in new ways to adapt to the changing environment and so on. The next stage input of the environment will then stimulate the N-FPGA transformation, which will then respond to the environmental change, which, in turn, will stimulate a transformation in the structural configuration of the N-EHW apparatus. This process of co-evolutionary transformation will continue to oscillate for numerous phases.

**[0093]** These co-evolutionary and adaptive processes will continue until optimal solutions are achieved. These complex dynamics of the N-EHW and N-FPGA systems will solve key molecular biology problems.

**[0094]** As the functional utility of the N-EHW operates in the environment, the structural apparatus of the N-EHW system will act upon and change the environment. The rate of change in the environment will therefore be reduced as the N-EHW performs its function, and thus the N-EHW and the N-FPGA interactions will achieve a relative position of equilibrium in the self-organizing and self-assembling systems.

**[0095]** Reference to the remaining portions of the specification, including the drawings and claims, will realize other features and advantages of the present invention. Further features and advantages of the present invention, as well as the structure and operation of various embodiments of the present invention, are described in detail below with respect to accompanying drawings.

**[0096]** It is understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims. All publications, patents, and patent applications cited herein are hereby incorporated by reference for all purposes in their entirety.

## **DESCRIPTION OF THE DRAWINGS**

**[0097]** FIG. 1 is a schematic diagram of a nano-scale integrated circuit.

**[0098]** FIG. 2 is a schematic diagram of an integrated circuit illustrating main sections.

**[0099]** FIG. 3 is a schematic diagram of a three dimensional nano-scale integrated circuit.

**[0100]** FIG. 4 is a diagram of a top view of the tiles of a nano-scale FPGA.

**[0101]** FIG. 5 is a schematic diagram of a four layer three dimensional nano-scale IC with fifteen sections on each layer.

**[0102]**FIG. 6 is a set of diagrams illustrating the sequence of an evolvable logic array.

**[0103]**FIG. 7 is a schematic diagram of a top view of a grid of evolvable logic gates shifting positions in a process of evolution.

**[0104]**FIG. 8 is a schematic diagram of a top view of an evolvable logic array illustrating the transformed position of the specific logic gates.

**[0105]**FIG. 9 is a schematic drawing of the top view of four layers of evolvable logic arrays in different positions.

**[0106]**FIG. 10 is a schematic drawing of the top view of an FPGA layer of an IC in the context of interaction with environmental change.

**[0107]**FIG. 11 is a flow chart showing the process of analyzing sensor data by an FPGA.

**[0108]**FIG. 12 is a flow chart showing the processing of an FPGA.

## **DETAILED DESCRIPTION OF THE DRAWINGS**

**[0109]**In order for nanorobots to have functionality, they require intelligence made possible by integrated circuitry. The three main models for semiconductors are application specific integrated circuits (ASICs), microprocessors (MPs) and complex programmable logic devices (CPLDs), the most prominent of which are field programmable gate arrays (FPGAs).

**[0110]**While most electronics IC components have grown to include billions of transistors, made possible by lithographic fabrication techniques to shrink the size of transistors, the present invention uses the development of nano-scale transistors to produce small nano-scale ICs. These minimalist ICs perform specific functionality associated with the first generation of useful MPs and ASICs, yet are in a tiny package that is integrated into nanorobotic apparatuses.

**[0111]**In addition to traditional two dimensional IC development, the present system also integrates the development of three dimensional ICs, which are more efficient and space saving than 2D components.

**[0112]**FIG. 1 illustrates the top view of a three dimensional nano-scale IC (100) which has a section for ROM (110) and RAM (120). The lines illustrate rows of transistors.

**[0113]**In FIG. 2, a top view of an IC (200) is illustrated with an emphasis on showing the sections of the layer of the IC. The RAM component (210) is shown and the multiply accumulate convert (MAC) component (220) is shown in differentiated sections.

**[0114]**FIG. 3 shows a three dimensional IC (300) with fourteen layers (310). 3D ICs provide a way to combine multiple layers for increased functional efficiency.

**[0115]**FIG. 4 shows a top view of the tiles on an FPGA layer (400). The outer layer shows 16 tiles (410) on which look up tables (LUTs) and ROM components are situated. The inner layer has 20 tiles (420) on which logic arrays are situated. The logic arrays have gates that change position to transform from one ASIC position to another in order to solve computational problems.

**[0116]**FIG. 5 shows an IC (500) comprised of a stack of four layers (510), with fifteen tiles on each layer (520).

**[0117]**FIGS. 6, 7 and 8 show the changed positions of the FPGA. FIG. 6 shows three main positions (A, B and C) illustrating the alternating positions of an evolvable logic array from position at 600 to position 610 to position 620. FIG. 7 shows the different positions of each layer (1 through 6 at 710 through 760) of a six layer FPGA (700). FIG. 8 shows a top view of a conversion process of a layer of an FPGA (800) as its logic array gates change from one position to another. In this dynamic sequence, the logic array gates continue to change their positions until they achieve the ASIC position. In some embodiments, this process of changing the position of gate arrays to various ASIC positions will continue until a computational problem is solved. In one view, this representation shows the cross section of the changing of a cellular automata process with each symbol referring to a temporary state feature (810, 820 and 830).

**[0118]**FIG. 9 illustrates the connection between four FPGAs (910, 920, 930 and 940) which are shown in different simultaneous positions.

**[0119]**FIG. 10 shows a top view of an FPGA layer (1000) with a reference to the changing environment. The FPGA will change positions in reaction to the changed inputs from the changing environment. At A (1010), an initial position will begin the process of changing the position state of the FPGA. As the environment changes (1050), the position B (1020) will alter the position of the gate array in the FPGA. This process continues as the environment

continues to change at C (1030) and D (1040). The changing of the positions of the FPGA gate arrays effectively reprograms the IC. As the chip is reprogrammed, it performs a new set of functions that interact with the environment. This interaction process provides a feedback loop.

**[0120]**FIG. 11 shows a flow chart which describes the initial process of repositioning the FPGA. After the power supply activates the IC (1100), software is loaded to ROM (1110) and sensors provide data inputs to the IC (1120). Data is transferred to the database in RAM (1130) and sensor data is analyzed by the IC (1140). Finally, the IC performs a function once activated by accessing the RAM (1150).

**[0121]**In FIG. 12, the process of FPGA operation is shown. Once the FPGA is activated (1200), software is loaded onto the look up tables (1210) and the logic array gates are activated (1220). Data is input to the FPGA (1230) and the FPGA processes the data in an initial position (1240). New data is input into the FPGA that requires a change of gate positions (1250) and the logic array gates move from position A to position B in a sequential process (1260). The process then repeats as new information is made available, which stimulates a transformation of the logic array gate positions. This process repeats until a specific problem is solved.

Patents by Neal Solomon

Patents by Neal Solomon



Patents by Solomon Research LLC

Patents in class PLA, PLD, FPGA, OR MCM

Patents in all subclasses PLA, PLD, FPGA, OR MCM

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**Patent Investment Trusts:  
 Let's Build a PIT to Catch the Patent Trolls**

*Elizabeth D. Ferrill<sup>1</sup>*

**troll** (trōl) *n.* In Norse Mythology, repulsive dwarfs who lived in caves or other hidden places. They would steal children and property but hated noise.<sup>2</sup>

**I. Introduction**

Peter Detkin, the assistant general counsel for Intel, coined the term "patent trolls" in the late 1990s, to describe his own impression of this new legal dwarf.<sup>3</sup> According to Detkin, a patent troll is "somebody who tries to make a lot of money off a patent that they are not practicing and have no intention of practicing and in most cases never practiced."<sup>4</sup> In a business that collects more than \$100 billion annually in licensing fees,<sup>5</sup> these patent trolls are taking an ever increasing piece of the licensing pie for themselves,<sup>6</sup> much to the chagrin of their prey.

<sup>1</sup> J.D. Candidate, University of North Carolina School of Law, 2006. Special thanks to Frank DeCosta, of Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. for his assistance.

<sup>2</sup> E.D. HIRSCH, JR. ET AL., *THE NEW DICTIONARY OF CULTURAL LITERACY* 45 (2002). "The troll in the children's story 'The Three Billy Goats Gruff,' for example, lives under a bridge and is enraged when he hears the goats crossing the bridge." *Id.*

<sup>3</sup> Brenda Sandburg, *Inventor's Lawyer Makes a Pile from Patents*, *THE RECORDER*, July 30, 2001, LEXIS, Nexis Library, RECRDR File.

<sup>4</sup> *Id.*

<sup>5</sup> Andrew Carter & Fayth A. Bloomer, *Generating Cash from a Patent Portfolio: An Overview*, *PAT. STRATEGY & MGMT.*, Aug. 6, 2004 at 5.

<sup>6</sup> Alexandra Dell, *Just Can't Get Enough*, *INTELL. PROP. L. & BUS.*, July 2004, available at <http://www.ipww.com/texts/0704/acadiz0704.html> (citing that Acacia Research Corporation's 2004 earnings are projected to be \$2.5 million, up from \$599,000 in 2003).

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